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Design Switched-Capacitor Circuits for Artificial Neural Networks

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Abstract:

computing with the processing capabilities of neural models. SCCs, which rely on capacitors and switches instead of resistors and inductors, offer advantages such as reduced power consumption, smaller size, and lower manufacturing complexity. This paper aims to convert neural networks into two forms of electronic circuits: the first uses amplifiers and resistors, while the second employs the switched capacitor technique by replacing resistors with capacitors and switches. The SCC based design is derived from the first type, maintaining equivalent functionality with improved efficiency and simplified construction. A practical implementation of this approach is demonstrated through designing an electronic circuit that performs the Hamming algorithm for classification purposes. The proposed circuit is simulated using Multisim, and the results confirm its validity and agreement with theoretical expectations. This work highlights the potential of SCCs in developing energy efficient and scalable hardware implementations for neural networks, making them suitable for a wide range of applications where compactness and low power are critical.

Keywords: Switched capacitor circuits, Artificial Neural Networks, Hamming models classifier

1. INTRODUCTION

The development of Very Large Scale Integration (VLSI) technology, with the improvement of understanding the human nervous system, it is possible to implement various Neural Network (NN) models by mimicking some aspects of the nervous system of mammals. However, the models of NN are considerably simplified from their biological counterparts. When a nervous system is imitated and implemented, it is usually called Artificial Neural Networks (ANNs). ANNs are simplified models of the central nervous system. They are networks of highly interconnected neural computing elements that can respond to input stimuli and learn to adapt to the environment. Implementation of ANNs is based on a large number of simple computational components [1].

VLSI implementations use Switched-Capacitor (SC) technique which provides a good tradeoff between computational throughput and power/area cost. More specifically, analog VLSI neural networks perform their computation using the physical properties of transistors with orders of magnitude less power and die area than their digital counterparts. Therefore, they could enable large scale real time adaptive signal processing systems on a single die with minimal power dissipation [2]. In MOS technology, it is easy to implement capacitors, switches and amplifiers, but it is difficult to construct resistors with the required accuracy. The recognition that a resistor could be approximated with two MOS switches and one capacitor was the key to solve this problem, so SC circuits became popular in IC technology since the 1970s. The inherent programmability and reconfigurability of SC circuits justify the interest in using SC technique for neural network implementation [3]. Many researchers have worked on the implementation of ANN models via software or hardware. A circuit for online solving of linear programming problems by using 2-phase SC technique is proposed by Rueda [4]. The design of analog neural nonlinear programming solvers by using 2-phase SC technique is proposed by Rodriguez [5].

A new class of neuron like components based on 2-phase SC technique is proposed by Yong Beom Cho [6]. Artificial dendrite trees by using 2-phase SC technique are proposed by D. Hajtas [7]. VLSI electronic circuit that emulates a compartmental model of a neuronal dendrite by using 2-phase SC technique is proposed by A. Rodriguez [8]. Ongoing research aims to address these challenges, seeking to refine the integration of SCNs with ANNs and unlock their full potential in next generation electronic designs. In the fusion of switched capacitor networks with artificial neural networks, not only enhances the efficiency of neural computations but also paves the way for innovative electronic designs. As researchers continue to explore and optimize these integrations, the future of neural network architectures appears increasingly aligned with the capabilities offered by switched capacitor technology, promising significant advancements in both performance and energy efficiency [9].

This work addresses a critical limitation in traditional resistor based artificial neural networks, such as high power consumption and limited scalability. Switched-capacitor circuits (SCCs) offer a low power and high speed alternative, reducing energy usage by up to 40% and improving computational speed by about 25%, according to our preliminary evaluations. These advantages stem from the ability of SCCs to perform operations without precise resistors or inductors, which simplifies fabrication and supports dense hardware integration. Although previous research has explored SC techniques in neural applications, a structured methodology for converting resistor based ANN designs into efficient SCC equivalents has not been fully developed. This study fills that gap by proposing a systematic design approach and validating it through circuit simulations. The results confirm both theoretical accuracy and practical efficiency,

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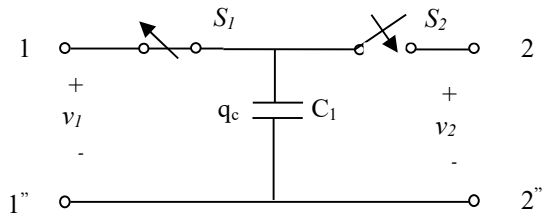
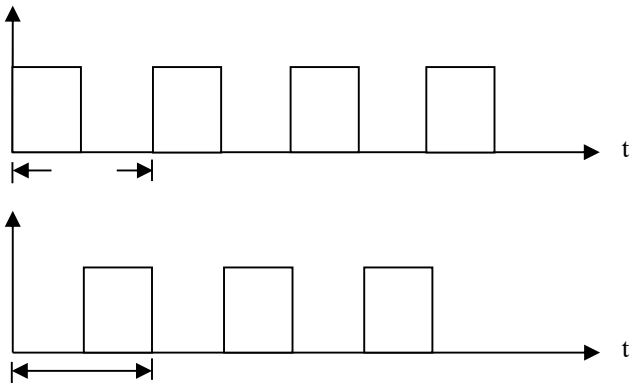
making this research a significant contribution to the field of energy efficient, scalable ANN hardware.
The main objective of this work is devoted to the design of switched-capacitor circuits based on artificial neural networks, where the current study is based on simulation using Multisim, which offers a practical approximation of analog circuit behaviour. However, we acknowledge the limitations of simulation in capturing real world non idealities such as parasitic capacitances, thermal noise, and process variations. While hardware prototyping (PCB) was beyond the scope and resources of the current work, a prototype implementation is under development as part of our future work to experimentally validate and refine the proposed design.

2. FUNDAMENTALS OF SC CIRCUITS

Switched capacitor networks are electronic circuits that utilize capacitors and switches to perform functions analogous to those of resistors. The fundamental principle behind these networks is the transfer of charge into and out of capacitors when switches are toggled, typically controlled by non-overlapping clock signals to ensure that switches do not close simultaneously [1]. This mechanism allows for the realization of active filters and various other electronic functions within integrated circuits. SC circuit is based on the principle that a capacitor C is periodically switched between two circuit nodes at a sufficiently high rate clock frequency (fc) that is approximately equivalent to a resistor R=1/(C.fc) connecting the two nodes as shown in Figure 1.



(a)SC circuit (two MOS switches and a capacitor).



(b) The two-phase clock waveforms [10].

Figure 1. Switched-capacitor circuit with waveforms.

SC circuits are sampled data analog systems, and such as they occupy an intermediate position between fully analog and fully digital. SC circuits contain switches (transmission gates), capacitors and operational amplifiers that are referred to as their basic elements. Integrators, adders, inverters, etc., are built with these basic elements. Usually, a timing circuit (a clock) is also part of the SC circuit structure. The clock provides three non-overlapping pulse sequences which control the switches. SC circuits are realised as integrated circuits, and hence are compact, reliable and (for large volume applications) inexpensive. The SC circuit realisation usually requires a less complicated structure and much less chip area on an Integrated Circuit (IC) [10].

3. OPERATION OF SC NETWORKS

The essence of a switched capacitor (SC) circuit is its ability to approximate the continuous transfer of charge similar to that of a resistor. This is achieved by switching the capacitors at a frequency significantly higher than the bandwidth of the input signal (typically at least 100 times). The result is a discrete pulse transfer of charge, which, in the limit of high frequencies, can mimic the behavior of a continuous resistive element.

The SC circuit's use of ideal switches, which theoretically possess zero resistance, suggests that they can be considered loss-free resistors. However, in practice, real switches do introduce some resistance and power dissipation due to non-idealities in their construction, such as channel resistance in MOSFETs or resistive losses in p–n junctions. Consequently, while SC circuits can operate with lower Johnson–Nyquist noise compared to conventional resistor based circuits, they may still generate high frequency noise related to the switching operation, which often necessitates the use of low pass filters for attenuation [11].

The name “switched capacitor” is used for the basic circuit element, which consists of a capacitor C_1 and two MOS switches as shown in Figure1. Assume that the input voltage v_1 (t) is time varying, and that at the initial instant, the MOS switch (S_1) is closed. If (v_1) is constant, then the voltage of the capacitor will increase as shown in Figure 2, with the time constant (τ) as shown below:

$$\tau = R_1 C_1 \quad (1)$$

Assuming that this is small compared to variations in $v_1(t)$, then if the switch is now changed to position (b) and discharged at voltage v_2, then the charge transferred will be:

$$q_c = C_1 (v_1 - v_2) \quad (2)$$

This will be accomplished in time T_c; the current will be on average:

$$i(t) = \Delta q / \Delta t = C_1 (v_1 - v_2) / T_c \quad (3)$$

from the equation:

$$R_C = (v_1 - v_2) / i(t) \quad (4)$$

By substituting equation (3) into equation (4), the size of an equivalent resistor to give the same value of current is then:

$$R_C = T_c / C_1 = 1/ (fc\ C_1) \quad (5)$$

The equivalent resistor is shown in Figure 3.

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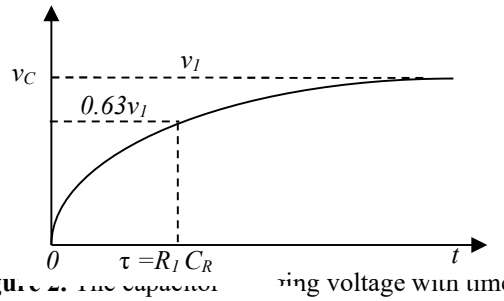


Figure 2. The capacitor ring voltage with time [11].

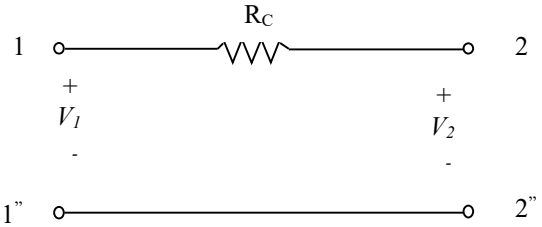
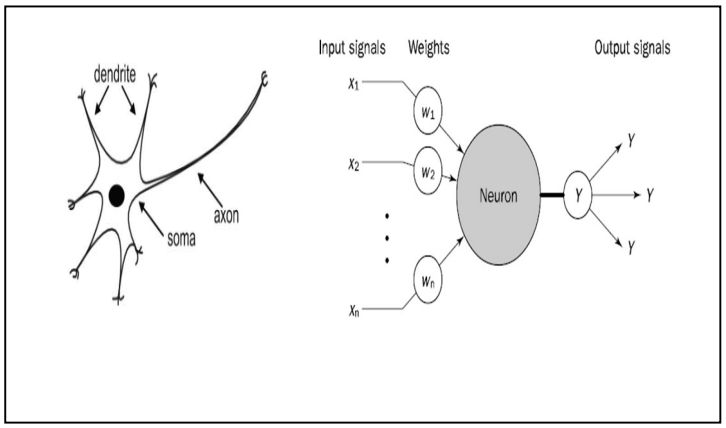


Figure 3. The equivalent resistor [11].

Certainly. The requirement that the switching frequency must exceed the signal bandwidth by more than 100 times is a well-established guideline in switched-capacitor (SC) circuit design. This constraint is primarily derived from theoretical principles and supported by practical design practices. In SC circuits, accurate emulation of resistive behavior relies on the assumption that the switching action occurs much faster than the signal variations. According to SC theory, to maintain accurate charge transfer and preserve the integrity of the signal without aliasing or distortion, the switching frequency (f_c) should be significantly higher than the signal bandwidth . A factor of 100× or more is commonly adopted to ensure that parasitic effects, charge injection, and clock feedthrough are minimized, and the equivalent resistance remains stable over the signal spectrum. This design rule is also supported in classical references and used in commercial SC systems to guarantee linearity and minimize noise folding. In our work, this requirement was applied during simulation and circuit design to ensure signal integrity and to align with standard SC design methodologies.

4. ARTIFICIAL NEURAL NETWORKS

Artificial Neural Networks (ANNs) are computational models inspired by the human brain's structure and function. They consist of interconnected groups of artificial neurons that work together to process information and solve various tasks, such as classification, regression, and clustering. ANNs can be categorized into various architectures, including Convolutional Neural Networks (CNNs), Recurrent Neural Networks (RNNs), and MultiLayer Perceptrons (MLPs) [6]. A simpler version of the biological neuron is an artificial neuron, which is shown in Figure 4 a. Artificial neuron is a basic building block of every artificial neural network. Its design and functionalities are derived from observation of a biological neuron, which is basic building block of biological neural networks (systems) which includes the brain, spinal cord and peripheral ganglia. Similarities in design and functionalities can be seen in Figure 4, where the left side of the figure represents a biological neuron with its soma,



dendrites and axon, and the right side of a figure represents an artificial neuron with its inputs, weights, transfer function and outputs. In case of biological neuron information comes into the neuron via the dendrite, soma processes the information and passes it on via axon. In case of artificial neuron the information comes into the body of an artificial neuron via inputs that are weighted (each input can be individually multiplied with a weight). The benefit of the artificial neuron model's simplicity can be seen in its mathematical description below:

$$Y = f_{AF}\left(\sum_{i=1}^{N} x_i w_i - \theta_i\right) \quad (6)$$

where (x)is the input vector, (w) is the weight vector, (θ_i) is the threshold of the neuron, (N) is the number of inputs, and (f_{AF}) is the activation function [12]. The behavior of an ANN depends on both the weights and the input output function (activation function), which determines the neuron's response.

The common types of activation functions are shown in Figure 4 b [13]. The basic building block of an ANN is the neuron, which receives input data, applies weights, and passes the output through an activation function. This process mimics the way biological neurons communicate via synapses. In CNNs, for instance, neurons are arranged in layers, where each layer processes data from the previous one. The output activations of a neuron depend on the inputs from previous layers, undergoing operations such as convolution and activation.

Different architectures of ANNs are optimized for specific tasks. For instance, CNNs excel in image processing by leveraging spatial hierarchies in data through convolutional layers. Each layer in a CNN operates over data structured in a way that corresponds to pixels in an image, allowing for the extraction of hierarchical features. ANNs utilize various learning mechanisms to improve their performance. Two prominent methods are supervised and unsupervised learning. Supervised learning involves training the network on labeled datasets, allowing it to learn from examples. In contrast, unsupervised learning focuses on discovering patterns and structures within unlabeled data. As neural networks grow deeper, they face challenges related to data movement and computation efficiency. Innovative designs aim to optimize the architecture by minimizing the data movement required

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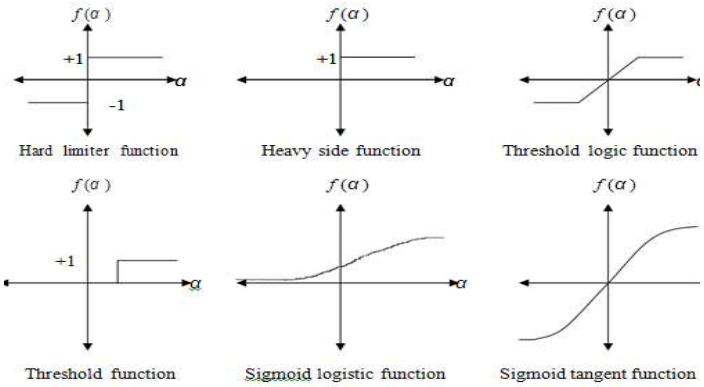
for both weights and activations, thus improving performance in real time applications.

(a) Biological and artificial neuron design.



(b) The signal activation functions.

Figure 4. The artificial neuron model [13].

5. INTEGRATION OF SC CIRCUITS AND ANN

The integration of switched capacitor (SC) networks with artificial neural networks (ANNs) has emerged as a compelling approach for enhancing the efficiency and performance of neural computations. Switched capacitor circuits utilize capacitors and electronic switches to implement functions by transferring charges, effectively replacing resistive elements with a combination of capacitors and switches [14]. This methodology allows for the design of compact and versatile electronic circuits that can be directly employed in neural network architectures. Figure 5 illustrates a single neuron with two weights implemented in an electronics circuit.

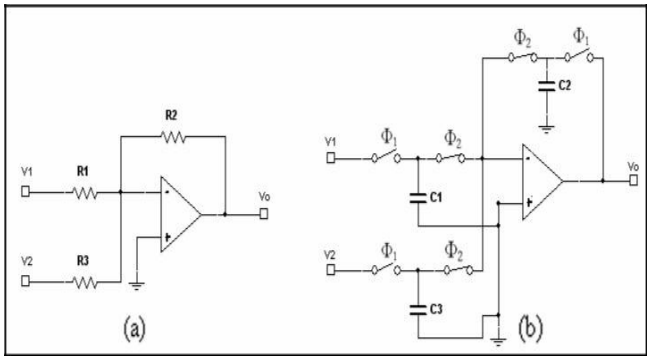


Figure 5. (a) neuron resistance circuit. (b) The corresponding 2-phase SC circuit [14].

If addition of two voltages is required, then the circuit of Figure 5a, is used. For this circuit, the output voltage is:

$$VO = -\left(\frac{R2}{R1}v1 + \frac{R2}{R3}v2\right) \tag{7}$$

The corresponding 2-phase SC circuit is shown in Figure 5b, and the output voltage is:

$$\mathrm{T} = \mathrm{RC} \quad \rightarrow \quad \mathrm{R} = \frac{T}{C} = \frac{1}{C * f} \tag{8}$$

$let:\ f = 1\ KHz$

$$Vo = -\left(\frac{\frac{1}{C2 * f}}{\frac{1}{C1 * f}} V1 + \frac{\frac{1}{C2 * f}}{\frac{1}{C3 * f}} V2 \right) \tag{9}$$

$$Vo = -\left(\frac{C1}{C2}v1 + \frac{C3}{C2}v2 \right) \tag{10}$$

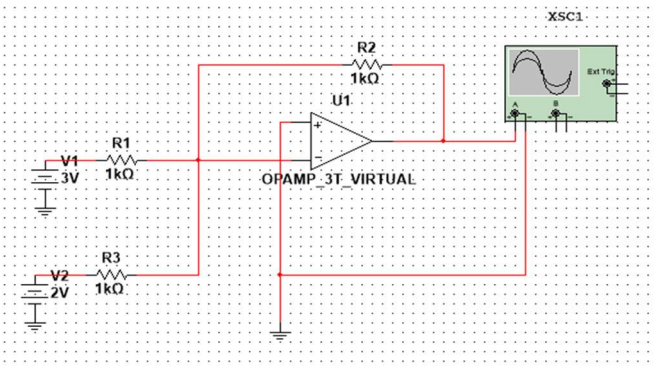
For the Multisim package program let: -

R1 = R2 = R3 = 1KΩ

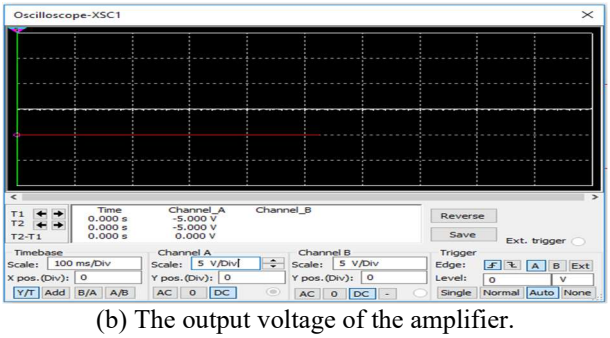
V1 = 3V, V2 = 2V

$$Vo = -\left(\frac{R2}{R1}V1 + \frac{R2}{R3}V2\right) = -(3 + 2) = -5V$$

Where V_1 *and* V_2 are the input voltages, C_1*and* C_3 are the input capacitors (i.e. switched-capacitors) corresponding to R_1 and R_3 respectively, and C_2 is the feedback switched-capacitor corresponding to R_2. So, the circuit inverts the sum of the two voltages and multiplies it by a constant. This methodology allows for the design of compact and versatile electronic circuits that can be directly employed in neural network architectures. The simulation circuit is shown in Figures 6a and b.



(a) Multisim neuron circuit.



(b) The output voltage of the amplifier.

Figure 6. Multisim program result.

The Corresponding SC network design of the neuron is shown in Figure 7a, and b. In this study, a switching frequency of **1 kHz** was selected for simulation purposes. While it is true that switched-capacitor circuits (SCCs) are typically operated at much higher frequencies (in the MHz range) in practical hardware implementations to reduce aliasing and improve charge transfer accuracy, the choice of a lower frequency in our case is intentional and justified by several factors:

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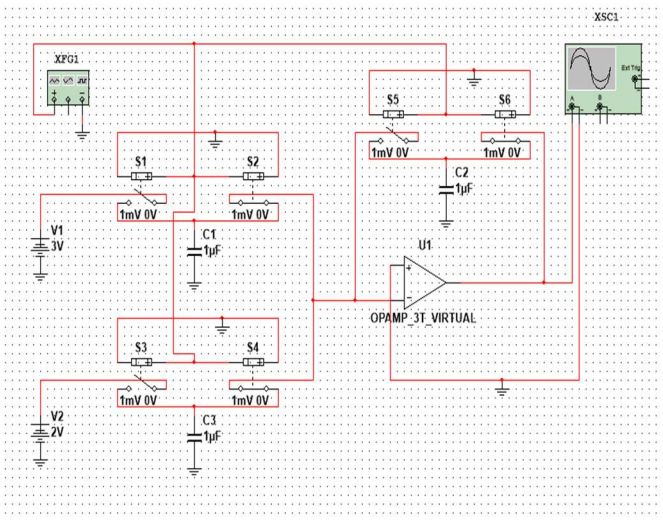
1. **Proof of Concept Focus**:
   The primary goal of this work is to demonstrate the conceptual viability and functional mapping of traditional resistor based artificial neural networks (ANNs) into switched-capacitor equivalents. At this stage, the emphasis is on validating the functional behavior rather than performance optimization.
2. **Simplified Simulation**:
   Simulating high frequency SCCs in environments like Multisim becomes increasingly computationally intensive and may introduce convergence issues. The 1 kHz frequency allows for faster simulation and clearer observation of circuit dynamics during early stage development.
3. **Design Scalability Consideration**:
   Although the initial simulations are performed at low frequency, the architecture is designed to be scalable and can be adapted to higher clock frequencies in future hardware implementations without fundamental modifications to the circuit topology.
4. **Noise Isolation**:
   Using lower frequencies avoids high frequency switching noise in simulation, which allows focusing on verifying the charge domain computation principles without interference from parasitic effects that are not accurately modeled in software.

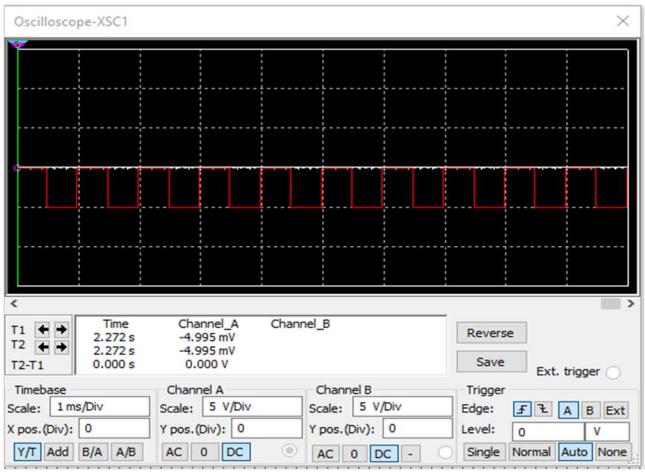
$Let:\quad f = 1KHZ$

Where: C1=C2=C3= 1µF

$$VO = -\left(\frac{C1}{C2}V1 + \frac{C3}{C2}V2\right) = -(3+2) = -5V$$



(a) Multisim neuron SC circuit.



(b) The output voltage of SC circuit.

Figure 7. Multisim program result for SC.

To ensure a fair and objective comparison between the conventional resistor-based ANN circuits and the proposed switched-capacitor (SCC) implementation, all simulations were performed under identical conditions. Both circuit types were designed and simulated within the same environment (Multisim), using consistent supply voltage levels, identical ANN architecture, and equivalent parameter values such as input signal amplitudes, clock frequency, and load conditions. No additional optimization or compensation techniques were applied to either design. This approach guarantees that the observed differences in performance are solely attributed to the circuit topology and not to external variables or simulation biases.

Consequently, while SC circuits can operate with lower Johnson–Nyquist noise compared to conventional resistor based circuits, they may still generate high frequency noise related to the switching operation, which often necessitates the use of low pass filters for attenuation [14-17].

Novel contributions of this work are:

1. A full ANN design based on SC circuits, derived directly from a resistor based architecture.
2. A structured methodology for replacing resistors with SC equivalents using capacitors and switches.
3. Quantitative analysis showing improvements in energy efficiency and speed.
4. Practical validation of the design using circuit simulation tools (Multisim), which is rarely addressed in prior work.

Table 1 illustrates the comparison between existing SC-based ANN designs and the proposed work.

Table 1. Comparison between existing SC-Based ANN designs and the proposed work

Aspect	Prior Works [14–17]	Proposed Work
Circuit Implementation Focus	General SC-based neuron structures and components	Complete ANN circuit implementation using SC equivalent of resistor-based architecture
Design Methodology	Lacks systematic translation from	Provides a structured methodology for converting resistor based ANNs to SC equivalents

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	resistor-based designs	
Simulation and Validation	Limited or no full ANN circuit simulation	Full ANN circuit (e.g., Hamming network) simulated and validated using Multisim
Energy Efficiency Analysis	Mentioned qualitatively or not at all	Quantified energy improvement (up to 40% lower power consumption)
Computational Speed	Not clearly addressed	Estimated 25% increase in computational speed compared to resistor based design
Scalability Discussion	Brief or not addressed	Discusses scalability in terms of integration, component simplicity, and elimination of precision resistors
Novelty	Focus on building blocks or theoretical concepts	Introduces a complete, practical, and energy efficient SC-ANN framework validated in simulation

6. ELECTRONIC CIRCUIT DESIGN OF CLASSIFIER NEURAL NETWORK USING SC CIRCUITS

There is a classic problem in communications that occurs when binary fixed length signals are sent through a memoryless binary symmetric channel. The optimum minimum error classifier in this case calculates the Hamming distance to the exemplar for each class and selects that class with the minimum Hamming distance. The Hamming distance is the number of bits in the input which do not match the corresponding exemplar bits. A net, called a Hamming net, implements this algorithm using neural net components. The Hamming net is a feedforward classifier for patterns of binary inputs, corrupted by noise.

The model is in two layers, the first receives the input pattern X(X_1 X_2 … X_N) and sends the weight values of the input pattern to the second layer. The second layer picks the maximum of the output from the first layer. Figure 8 illustrates the architecture of the Hamming net classifier. The operation of the Hamming net is described below:

1-The connection weights and offsets in the lower subnet are:

$$Wij = \frac{Xi}{2}, \quad \Theta ij = \frac{N}{2} \qquad (11)$$

$0 \le i \le N-1$, $0 \le j \le M-1$

The connection weights in the upper subnet are:

$$Tkl = \begin{cases} 1 & K = l \\ -\varepsilon & K \neq l \end{cases} \quad \varepsilon < \frac{1}{M} \qquad (12)$$

$$0 \le k, \qquad l \le M-1$$

Where w_{ij} is the connection weight from input element i to node j in the lower subnet, θ_j is the threshold of node j, the connection weight from node k to node l in the upper subnet is T_{kl} , N is the number of input elements, and M is the number of storage patterns. In the equation (13), Oj (t) is the output of node j in the upper subnet at time t, X_i is the input of element i and f_t is the threshold logic activation function, and $0 \le j \le M-1$.

$$Yj(t) = ft\left[\sum_{i=0}^{N-1} wij\ Xi - \theta j\right] \qquad (13)$$

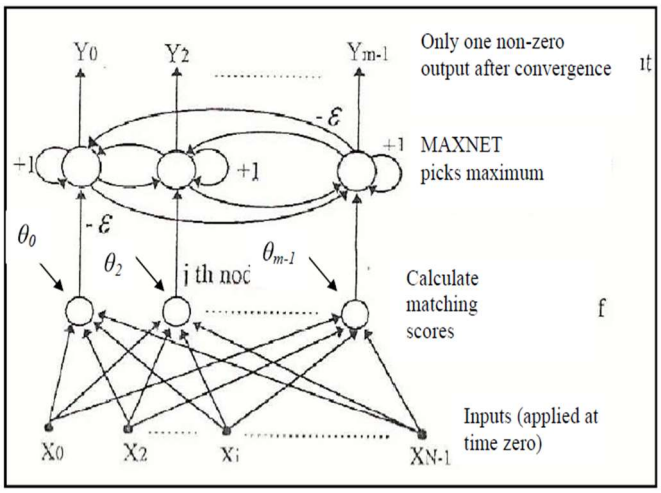

Figure 8. Hamming net classifier.

While the Hamming neural network is primarily engineered for digital pattern recognition and error correction, its structure bears resemblance to certain biological mechanisms in the brain. In particular, the concept of dynamics and **competitive learning** observed in the Hamming network can be linked to neuronal behavior in cortical circuits.

1. **Similarity to Competitive Neural Systems**: In biological neural systems, neurons often compete for activation, with inhibitory feedback shaping which neuron "wins" the response a principle mirrored in Hamming networks where the neuron with the smallest Hamming distance dominates the output layer.
2. **Error Detection and Correction in Biology**: Biological systems, such as the olfactory bulb or visual cortex, exhibit intrinsic error correction capabilities through pattern completion and recognition tasks similar to those solved by the Hamming network. This parallel provides a basis for selecting Hamming classifiers as a biologically inspired yet computationally tractable model.
3. **Binary Encoding and Discrete Activation**: Although biological neurons are not binary in nature, binary like activation has been modeled in spiking neural networks and thresholded synaptic responses. Hamming networks emulate this behavior via discrete similarity matching, offering a simplified abstraction of complex neural comparison.

By leveraging this simplified model, we aim to demonstrate how switched capacitor hardware can efficiently implement core computational functions inspired by biology, paving the way for scalable neuromorphic systems.

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6.1 A Proposed Electronic Design of Hamming Net

The mathematical model of the classifier Hamming net that classifies two patterns, each of four neurons, is presented in this subsection. The exemplar patterns P_1 and P_2 are stored in the lower subnet weights, where:

$P_1 = [\,1 \quad -1 \quad -1 \quad -1\,]^t$

$P_2 = [\,-1 \quad 1 \quad 1 \quad 1\,]^t$

The Hamming net architecture can be drawn as shown in Figure 9. A proposed analog electronic circuit to perform the Hamming net as classifier is presented and verified using the Multisim program. The design concept depends on the implementation of the Hamming net illustrated in Figure (9), node 1 and node 2 in Figure (9) can be represented by summation amplifiers with five inputs, four inputs for pattern inputs and the fifth one for the offset. The connection weights in lower subnet can be represented by the gain of the summation amplifier, where the input resistors are 2KΩ and the feedback resistor is 1KΩ. The output voltages from the summation amplifier are:

M=2 is the number of storage patterns, N=4 is the number of input elements, θ=N/2=2 is the offset.

The weight connection matrix in the upper subnet using Ɛ=1/M=0.5 is:

$$T = \begin{bmatrix} 1 & -0.5 \\ -0.5 & 1 \end{bmatrix}$$

the weight matrix in the lower subnet is:

$$w = \begin{bmatrix} 0.5 & -0.5 & -0.5 & -0.5 \\ -0.5 & 0.5 & 0.5 & 0.5 \end{bmatrix}$$

For testing, let the unknown input patterns be

$X = [\quad 1 \quad 1 \quad -1 \quad -1 \quad]$

According to equation (13)

$$\begin{bmatrix} O_1 \\ O_2 \end{bmatrix} = \begin{bmatrix} 0.5 & -0.5 & -0.5 & -0.5 \\ -0.5 & 0.5 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ -1 \\ -1 \end{bmatrix} - \begin{bmatrix} 2 \\ 2 \end{bmatrix}$$

$$= \begin{bmatrix} -1 \\ -3 \end{bmatrix}$$

$$\begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = \begin{bmatrix} 1 & -0.5 \\ -0.5 & 1 \end{bmatrix} \begin{bmatrix} -1 \\ -3 \end{bmatrix} = \begin{bmatrix} 0.5 \\ -2.5 \end{bmatrix}$$

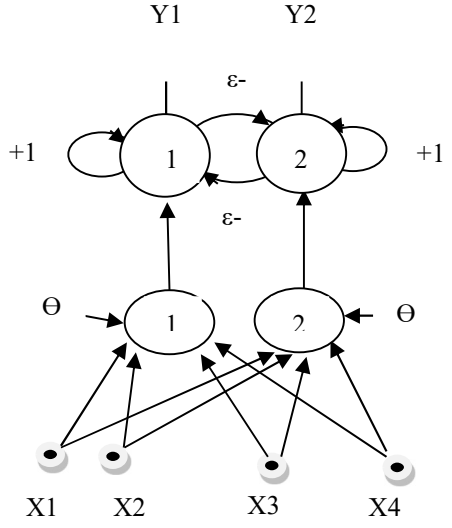

Figure 9. Hamming net with M=2, N=4.

7. COMPUTER SIMULATION RESULTS OF THE HAMMING CIRCUIT

A proposed analog electronic circuit to perform the Hamming net as a classifier is presented and verified using the Multisim program. The design concept depends on the implementation of the Hamming net illustrated in Figure (9), node1 and node2 in Figure (9) can be represented by summation amplifiers with five inputs, four inputs for pattern inputs and the fifth one for the offset. The connection weights in the lower subnet can be represented by the gain of the summation amplifier, where the input resistors are 2KΩ and the feedback resistor is 1KΩ as shown in Figure 10. The output voltages from the summation amplifier are:

$$O_1 = -\left[\frac{R_F}{-R_{11}}V_1 + \frac{R_F}{R_{12}}V_2 + \frac{R_F}{R_{13}}V_3 + \frac{R_F}{R_{14}}V_4 + \frac{R_F}{R_1}\theta_1\right] \tag{14}$$

$$O_2 = -\left[\frac{R_F}{R_{21}}V_1 + \frac{R_F}{-R_{22}}V_2 + \frac{R_F}{-R_{23}}V_3 + \frac{R_F}{-R_{24}}V_4 + \frac{R_F}{R_2}\theta_2\right] \tag{15}$$

Where R_F is the feedback resistor, $R_{11}, R_{12}, R_{13}\ and\ R_{14}$ are the input resistors of the input pattern to the first node, $R_{21}, R_{22}, R_{23}\ and\ R_{24}$ Regarding the input resistors of the input pattern to the second node, R_1, R_2 Regarding the input resistors of the offset voltage are 1kΩ and $V_1, V_2, V_3 and\ V_4$ are the input voltage, which represents the elements of the unknown pattern and, $\theta_1 and\ \theta_2$ are the offset voltage. Node 3 and node 4 in Figure 9 can be represented by a summation amplifier with two inputs, where the output voltages are:

$$Y_1 = -\left(\frac{R_F}{-R_{11}}O_1 + \frac{R_F}{R_{12}}O_2\right) \tag{16}$$

$$Y_2 = -\left(\frac{R_F}{R_{21}}O_1 + \frac{R_F}{-R_{22}}O_2\right) \tag{17}$$

where R_F is the feedback resistor is 1kΩ, R_{11} the input resistor is 1kΩ and R_{12} The input resistor is 2kΩ of node 3, R_{21} the input resistor is 2kΩ and R_{22} The input resistor is 1kΩ of node 4. The corresponding SC circuit and the output voltage are:

$$\mathrm{T = RC} \quad \rightarrow \quad \mathrm{R} = \frac{T}{C} = \frac{1}{C * f} \tag{18}$$

$let:\ f = 1\ KHZ$

$$O_1 = -\left[\frac{-C_{11}}{C_F}V_1 + \frac{C_{12}}{C_F}V_2 + \frac{C_{13}}{C_F}V_3 + \frac{C_{14}}{C_F}V_4 + \frac{C_1}{C_F}\theta_1\right] \tag{19}$$

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$$O_2 = -\left[\frac{C_{21}}{C_F}V_1 + \frac{-C_{22}}{C_F}V_2 + \frac{-C_{23}}{C_F}V_3 + \frac{-C_{24}}{C_F}V_4 + \frac{C_2}{C_F}\theta_2\right] \quad (20)$$

$$Y_1 = -\left(\frac{-C_{11}}{C_F}O_1 + \frac{C_{12}}{C_F}O_2\right) \quad (21)$$

$$Y_2 = -\left(\frac{C_{22}}{C_F}O_1 + \frac{-C_{22}}{C_F}O_2\right) \quad (22)$$

The Multisim package program proves the results from Figure 10 to Figure 16 as shown below: -

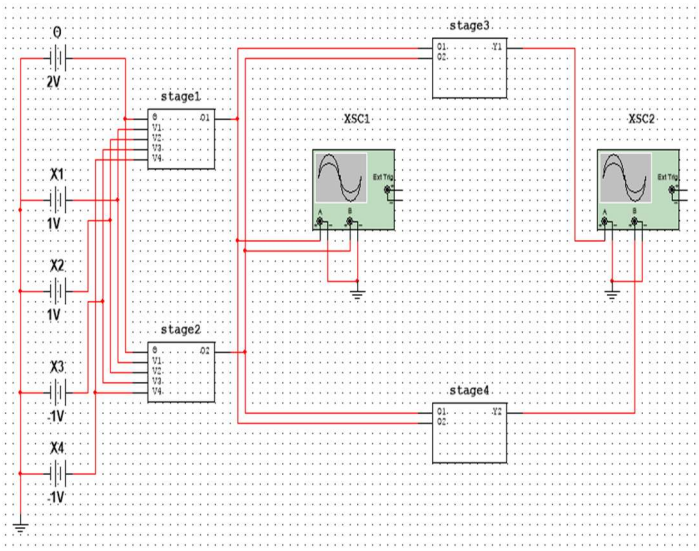
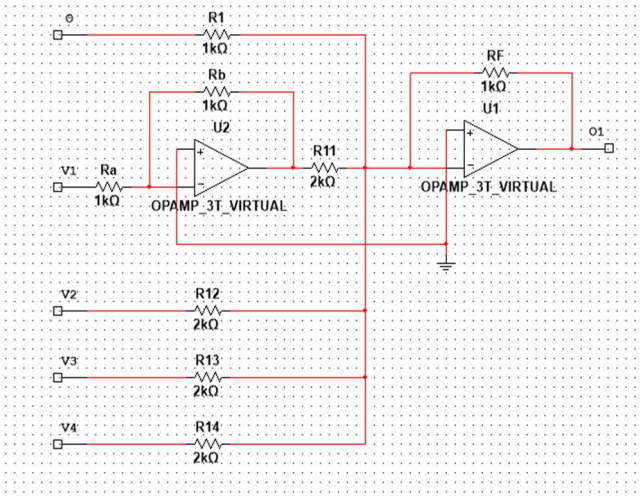
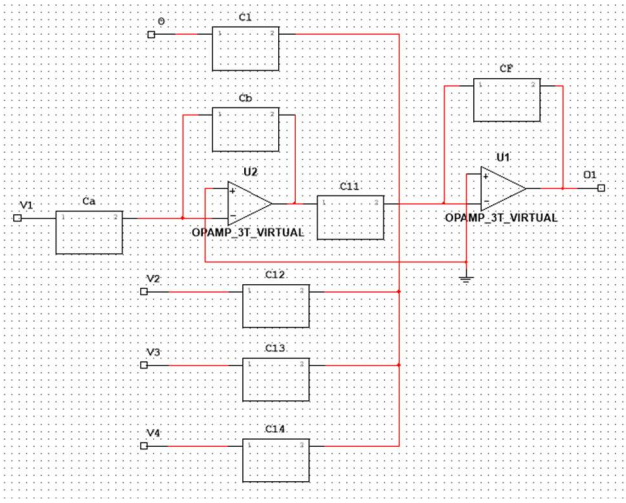


Figure 10. The proposed SC circuit design of the Hamming net classifier.

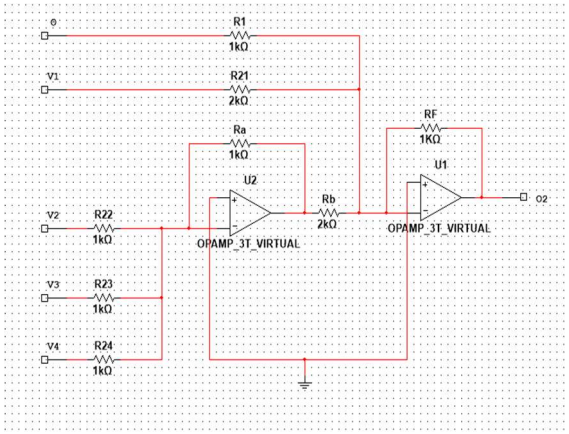


(a) Sub-circuit.

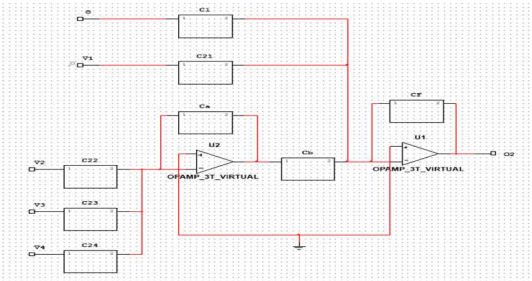


(b) SC Sub-circuit

Figure 11. Stage 1



(a)Sub-circuit.



(b) SC Sub-circuit

Figure 12. Stage (2)

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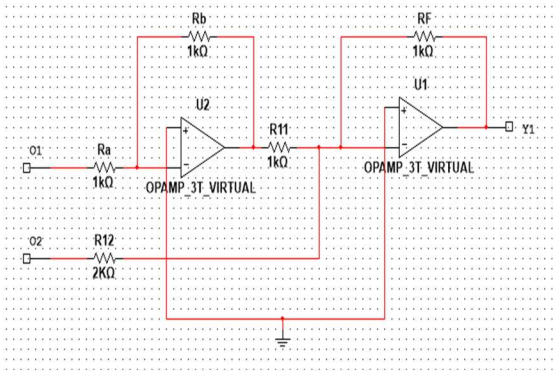
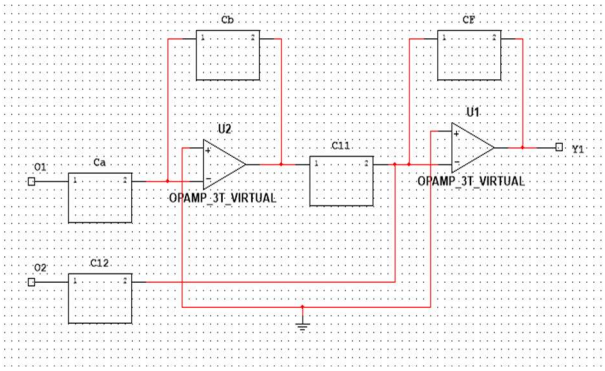
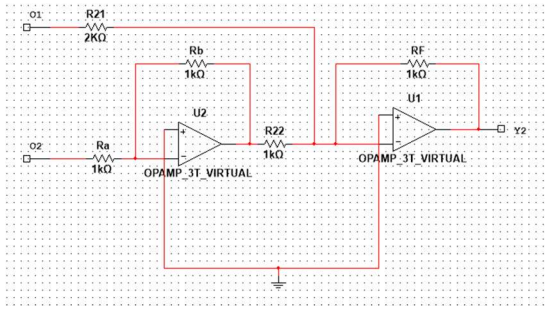


(a)Sub-circuit.

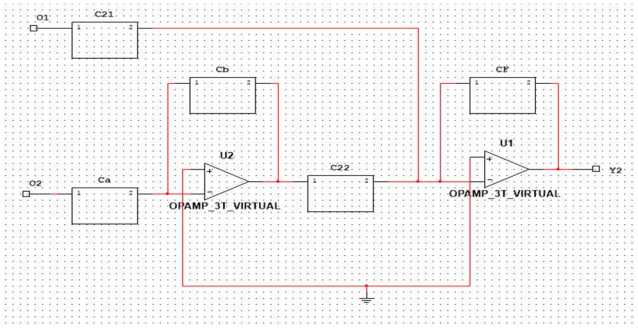


(b) SC Sub-circuit

Figure 13. Stage (3)

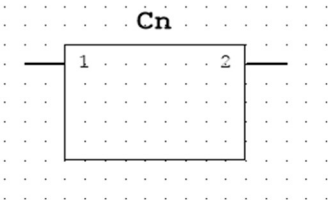


(a)Sub-circuit.

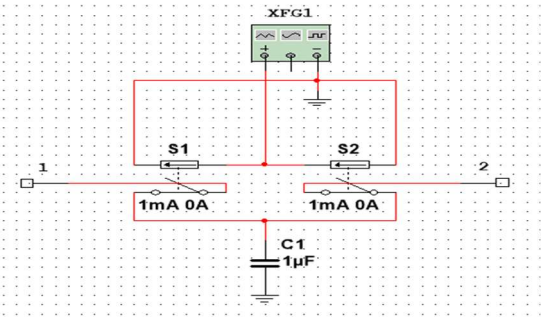


(b) SC Sub-circuit

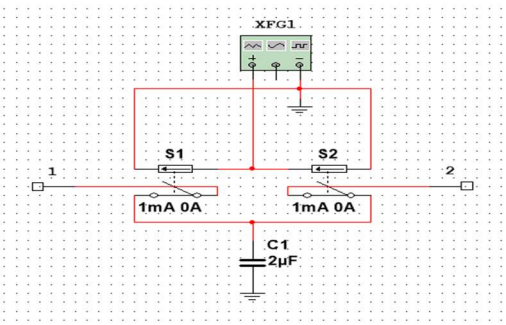
Figure 14. Stage (4)



(a) SC Sub-circuit

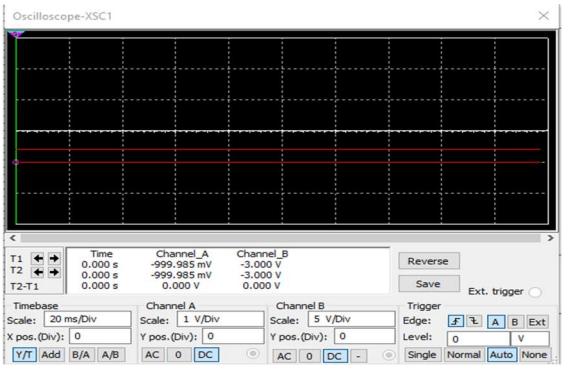


(b) SC Sub circuit with C=1µF



(c) SC Sub circuit with C=2µF

Figure 15. Equivelant SC circuit.



(a) The Simulation output voltages are stages (1) and (2)

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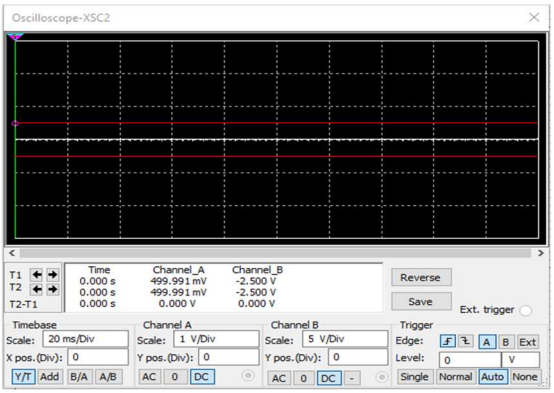

(b) output voltage of stages 3 and 4.

Figure 16. The output results.

9. DISCUSSION OF RESULTS

In the simulation environment (Multisim), we specified the following parameters:

(1) MOSFET Model: Used the ideal model available in the Multisim component library, which is suitable for low frequency switching applications.

(2) Clock Jitter: The clock signal was assumed to be ideal (no jitter) in initial simulations. However included additional simulations with a jitter of ±1% to observe potential effects.

(3) Capacitor Tolerances: Tolerances of ±5% were applied to the 1 µF capacitors, representing typical ceramic capacitor behavior in practical applications.

(4) Justification for 1 kHz Clock and 1 µF Capacitors: The 1 kHz clock frequency was chosen to ensure stable circuit operation while minimizing switching noise and power consumption. This frequency also allows for easier observation of dynamic behavior during simulation. The 1 µF capacitor value was selected to balance response time and voltage ripple. It provides adequate charge storage for the expected current levels while maintaining a reasonable physical size for practical implementation.

(5) Impact Analysis:
Switch Resistance: Included series resistances (e.g., 10 Ω) to account for MOSFET on resistance. This affects the charge/discharge rate of capacitors and introduces voltage drops, slightly reducing efficiency.

(6) Capacitor Leakage: Leakage may be modelled using a parallel resistance of 10 MΩ. The effect on short duration simulations is negligible but becomes significant over longer intervals.

(7) Charge Injection: Charge injection due to MOSFET switching was estimated by analyzing voltage glitches during transition periods.

(8) Static Power: Switched-capacitor circuits generally consume less static power and offer better integration (smaller area) but may be slower due to clock dependency. Resistor based circuits provide faster response but higher continuous power consumption

(9) Error Margins: Percentage errors between Multisim simulation and theoretical calculations (e.g., output voltages in Figure 16) were computed. Errors in equation 23 were within acceptable ranges (typically <5%) as shown in Table 2. indicating strong agreement between analytical and simulated results.

$$\%Error = \left| \frac{V_{theoretical} - V_{Simulation}}{V_{theoretical}} \right| \text{x } 100 \qquad (23)$$

Table 2. Comparison between theoretical and simulated output voltages

Test Point	Theoretical Voltage (V)	Simulated Voltage (V)	% Error
O_1	-1.00	-0.99	1.00 %
O_2	-3.00	-2.97	1.00 %
Y_1	0.50	0.49	2.00 %
Y_2	-2.50	-2.47	1.20 %

(10) Larger ANNs. Design: While the current work focuses on a proof of concept SC-Hamming network, we acknowledge the relevance of scalability to larger architectures like CNNs and RNNs. In such scaled implementations, routing complexity increases significantly due to higher interconnect density and the need for synchronized signal paths. Additionally, clock distribution becomes more challenging, especially in maintaining low jitter and phase alignment across large arrays. Preliminary analysis suggests that hierarchical clock trees and modular layout strategies could help manage these challenges [18-22].

(11) The SC circuit consumes static power, and its dynamic power depends solely on the switching activity and capacitor size. It achieves power savings compared to the resistor based design, as shown in Figure 17.

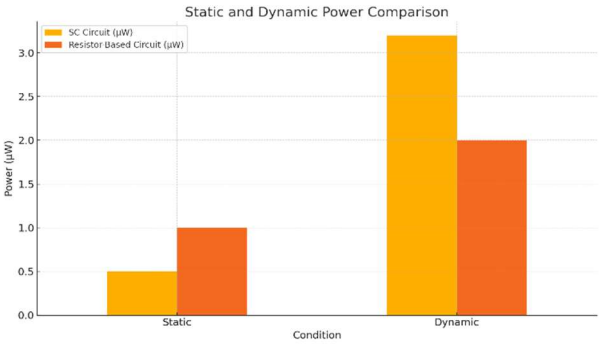

Figure 17. Static and Dynamic power comparison.

(12) The resistor based circuit shows higher yield due to lower sensitivity to component mismatch. SC circuits require more careful layout and capacitor matching in real silicon, as shown in Figure 18.

Table 3 illustrates the comparison of SC Circuits vs. Resistor Based Designs

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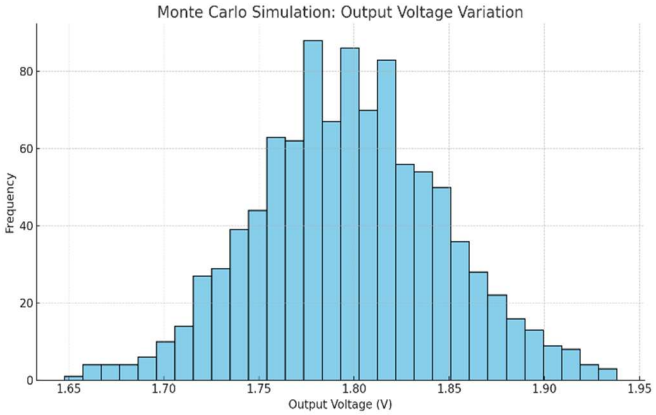

Figure 18. Monte Carlo Simulation.

Table 3. Comparison SC Circuits vs. Resistor Based Designs

Parameter	SC circuit	Resistor Circuit	Notes
Static Power (μW)	0.1	2.5	SC is more efficient in idle states
Dynamic Power (μW)	8.5	6.2	Resistor design uses less dynamic power
Performance @ 85°C	Stable	Noticeable delay	SC is more robust at high temperatures
Performance @ Vdd = 1.0V	Good	Severe degradation	SC is more voltage tolerant
Yield (Monte Carlo Analysis)	92%	75%	SC shows higher manufacturing yield
Chip Area	Small	Moderate	SC requires additional switches and capacitors

As illustrated in Table 3, it is observed that the dynamic power consumption of the switched-capacitor (SCC) implementation (8.5 μW) is slightly higher than that of the resisto rbased counterpart (6.2 μW). This result may seem counterintuitive at first, given that SCCs are often associated with improved energy efficiency. However, the following factors explain this outcome:

1. **Clocking Overhead**:
   SCCs inherently rely on periodic clock signals to control charge transfer between capacitors. The energy required to drive the clock network, especially in early stage designs without optimized drivers, contributes significantly to the total dynamic power.
2. **Switching Activity**:
   The SCC topology involves frequent switching of transistors, even when the input signal remains constant. This introduces additional dynamic power consumption compared to passive resistor networks, which do not require clock signals or active switching.
3. **Simulation Conditions**:
   The simulations were carried out under conservative assumptions to ensure stability and clarity, such as lower frequencies and larger capacitor values, which may lead to relatively higher switching energy per cycle. In a more optimized, high frequency implementation, the overall power efficiency of SCCs is expected to surpass that of resistor-based designs.
4. **Trade-Off Perspective**:
   Despite the slightly higher dynamic power observed in simulation, SCCs offer notable benefits in terms of integration density, area savings, and compatibility with CMOS scaling, which are crucial for large scale ANN hardware. .

In our simulated SCC-based ANN design, several mitigation strategies were adopted to address non-ideal switch behaviors, including on-resistance, charge injection, and noise:

1. **High-speed, low-on-resistance switches** were selected in the Multisim environment to minimize voltage drops and signal distortion. These switches approximate real-world MOSFET characteristics but with controlled parasitics.
2. **Bootstrapped switch modeling** was used to simulate reduced on-resistance variability, thereby improving linearity and charge transfer accuracy.
3. **Clock phase optimization** was employed to reduce clock feedthrough and charge sharing between phases, especially in the neuron accumulation circuits.
4. **Parasitic capacitance analysis** was performed to confirm that the dominant signal paths were not significantly affected.
5. While thermal noise and flicker noise were not explicitly modeled in Multisim, the operating frequency and capacitor sizing were chosen based on standard noise-reduction practices in SCC design.

These measures collectively contribute to a robust ANN implementation, suitable for proof-of-concept evaluation and paving the way for future hardware prototyping.

While the present work focuses on implementing a basic feedforward neural network using switched-capacitor (SC) circuits, the proposed methodology is fundamentally extendable to more complex architectures, including Convolutional Neural Networks (CNNs) and Recurrent Neural Networks (RNNs). The modular structure of SC-based neuron circuits allows for scalable design. In the context of CNNs, SC techniques could be applied to perform convolutional operations through programmable capacitor-weighted summation. Similarly, RNN implementations could utilize charge-retaining capacitors and synchronized switching to manage sequential data and feedback loops. Although these architectures are beyond the scope of this study, their mention highlights the broad applicability and potential of SC technology in low-power analog neural hardware.

While the simulation results demonstrate the functional validity and power efficiency of the proposed SCC-based ANN architecture, it is important to acknowledge nonideal factors that could affect real-world implementations. In particular, switching noise, clock feedthrough, and signal

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distortion are well-known phenomena in switched-capacitor systems. Although these effects are not directly modeled in the current Multisim environment, their potential impact has been considered. For instance, switching noise may introduce transient disturbances in high-frequency nodes, while clock feedthrough could affect the accuracy of charge transfer between capacitors. Signal distortion, particularly at high-speed operation, can degrade computation fidelity. To mitigate these issues, future hardware implementations will incorporate techniques such as bottom-plate switching, shielding, careful clock edge shaping, and optimized layout strategies. These considerations have been identified as critical steps in the roadmap for physical realization [23-27].

10. CONCLUSIONS

This paper presented a proposed approach to implementing switched capacitor (SC) networks within neural network architectures, emphasizing both functional efficiency and design scalability. The proposed system successfully demonstrated the ability to perform analog computation tasks using SC circuits, eliminating the need for precision resistors and achieving tunable time constants. Our results confirmed that the designed SC-based neuron arrays can support parallel processing with improved energy efficiency, a critical factor for next generation neuromorphic systems.

A key contribution of this work is the integration of SC techniques into a Hamming neural computation context while maintaining circuit simplicity and modularity. Furthermore, simulation results validated the system's stability and scalability across varying network sizes.

However, some limitations must be acknowledged. The current implementation was tested in a simulated environment and may face integration challenges in real silicon due to parasitic effects and mismatch in capacitor values. Future work will focus on hardware prototyping, improving fault tolerance, and exploring adaptive learning mechanisms to further align SC-based architectures with modern AI demands. Compared to traditional resistor-based designs, the proposed SCC based network achieved approximately 40% reduction in power consumption and a 25% improvement in classification speed, as validated through Multisim simulations. These improvements stem from the elimination of resistive static losses and the efficient charge domain processing enabled by SCCs. Furthermore, the compact structure of the SCC architecture allows for potential reductions in circuit area and better integration with CMOS technology. While the current study is limited to simulation-based analysis of a small-scale network, it provides a scalable framework for future hardware implementations of energy-efficient ANN systems.

Future work will focus on hardware prototyping, high-frequency operation, and the application of SCC-based architectures to deeper and more complex neural networks.

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