Design And Implementation of 32 x 32 SRAM For Low Power Applications

Dr. Katragadda Swarnasri[#1], Asanapuram Vasantha [*2], Kandagunta Tirumala rao[#3], Karri Udaya sri[#4], Devarakonda Varshitha joy[#5]

[#1]*Professor, Department of EEE R.V.R & J.C College of Engineering (Autonomous), Chowdavaram, Andhra pradesh, India.*

[*2, #3, #4, #5] *Student, Department of EEE R.V.R & J.C College of Engineering (Autonomous) ,Chowdavaram, Andhra pradesh, India*

[1]swarnasrik@gmail.com, [2]vassumallikarjuna48@gmail.com .

ABSTRACT

Static Random Access Memory (SRAM) is an essential element in current digital systems which is extensively utilized in cache memory and low power applications owing to its high-speed and reliability features. With the development of the CMOS technology, the amount of leakage power has turned into one of the most dominant factors causing total power dissipation, especially at standby mode. This paper focuses on designing and implementation of a low power 32x32 SRAM memory array by applying the power gating scheme in order to overcome the leakage power issue. The proposed architecture is comprised of conventional 6T SRAM cells along with sleep transistors capable of turning off power to the memory arrays during stand-by mode. In order to validate the performance of the proposed circuit, Tanner EDA software packages such as S-Edit for schematic drawing and T-Spice for simulation are employed. The comparison between the proposed and traditional designs reveals that the power consumption is considerably decreased from 2.615 µW to 1.7402 µW while increasing the number of transistors slightly.

Keywords: SRAM Memory, 6T SRAM Cell, Low Power Design, Power Gating Technique, Leakage Power Reduction, Tanner EDA, CMOS Technology, Memory Array Design

I. INTRODUCTION

Static Random Access Memory (SRAM) is considered one of the vital components that are commonly applied in the development of digital circuits because of their fast speed, short access time, and easy implementation using CMOS technologies. Over the last few decades, the demand for low power memory structures has seen a tremendous rise because of the advancement of portable and battery-operated gadgets, including medical implantable devices, wearable devices, and IoT.

With the further miniaturization of CMOS technology to the nano-scale level, power dissipation has become an important consideration in designing chips. Power dissipation in SRAMs can be categorized into two types: dynamic power dissipation and static power dissipation. Although dynamic power consumption occurs due to switching actions, static power dissipation happens when there is no switching action in the circuit. As the technology scale down, the static leakage currents in transistors become more prominent in deep submicron technology because of a lower threshold voltage, subthreshold leakage, and tunneling through the gate oxide effect. A standard SRAM cell design usually uses a 6-transistor (6T) design, where each cell comprises two cross-coupled inverters along with two access transistors. Despite having a good trade-off among performance, stability, and efficiency, the 6T SRAM cell is prone to substantial power leakage. In large SRAM memory arrays, such as the 32×32 SRAM array cell design, the accumulated leakage power of thousands of transistors becomes high enough, making it inefficient in low-power applications without employing other power-saving methods.

In an effort to solve the above problem, there are several existing power-saving approaches that can be employed, some of which include transistor sizing optimization, voltage scaling, MTCMOS design, and utilizing other types of SRAM cells such as 8T, 9T, and 10T designs. While these methods enable saving on power and increase stability, they also pose some challenges, which include increasing the overall design area, increasing complexity, and decreasing performance. This makes it necessary for the development of another effective power reduction technique without much design overhead. Power gating has recently been considered as a potential means of achieving leakage power saving in VLSI designs. In power gating, high threshold voltage sleep transistors are used to gate the power supply rails to the circuits to be disconnected from their sources during idle periods, hence saving on the leakage power without affecting the functionality of the circuit when it is in operation.

In this project, a 32×32 SRAM memory array that uses power gating to save on leakage power has been designed and implemented. Sleep transistors have been used in combination with the standard 6T SRAM array structure to provide minimal leakage power when the array is in an inactive state. The design includes important elements such as row and column decoders, sense amplifiers, and precharge circuits to enable proper read/write operations. Modeling and simulation of the entire array circuit have been done using Tanner EDA software packages such as S-Edit, T-Spice, and W-Edit. Main contributions of this paper include the following:

(i) development of a 32x32 SRAM array based on traditional 6T cells,

(ii) inclusion of power gating scheme for leakage power minimization,

(iii) performance analysis by means of simulation using Tanner EDA software tool, and

(iv) comparison indicating a considerable power saving along with minor hardware complexity.

As the simulation results confirm, the designed SRAM circuit offers considerable power saving over the traditional SRAM without compromising on performance and reliability. Therefore, the designed SRAM is appropriate for low power application scenarios.

II LITERATURE SURVEY

In light of the growing trend towards developing memory systems that consume less power yet operate with high speed, various research studies have emerged in order to enhance the performance of the SRAM architecture. Several methods have been proposed in order to overcome problems related to the scaling of SRAM circuits, which include leakage power, instability, and degradation of performance.

Calhoun and Chandrakasan studied the effect of **scaling the supply voltage** of the SRAM on stability, and they looked at how the SNM varies as the SRAM operates below its threshold voltage. Their results suggest that although scaling voltage decreases dynamic power, it negatively impacts the SRAM circuit in terms of stability, hence affecting its reliability.

The concept of **near-threshold** computing was examined by **Dreslinski et al**. as an effective way to conserve energy during the execution of computation tasks. They showed that near threshold voltages lead to a significant decrease in power, but it causes other problems like delay and variation. A new 10T SRAM cell structure was introduced by Chang et al., to achieve read stability and minimize leakage power. The separation between read and write operations makes the design more stable, but with an increase in transistors, this SRAM cell increases the silicon area and becomes difficult to scale.

Pasandi et al. introduced a novel 9T SRAM cell structure, focusing on enhancing the stability of the design and minimizing leakage current problems. While the design is more efficient than the traditional 6T SRAM cell, more circuitry is required to implement the structure.

In addition to various SRAM cell designs, there have also been other approaches to leakage minimization. Two such techniques are MTCMOS and transistor stacking. However, despite all these developments, there is still a trade-off that needs to be addressed, especially in SRAM cell design, in which the increase in the number of transistors enhances the stability and reduces the leakage but at the expense of area and scalability, especially in large SRAM arrays such as 32×32 SRAM.

A way to solve this problem is to adopt a new power-efficient technique known as power gating. By using sleep transistors to effectively disconnect unused memory cells from power supplies, power gating ensures that a significant amount of leakage power is saved while the rest of the advantages offered by 6T SRAM cell remain.

It is against this backdrop that the current research project will be concentrating on applying the power gating technique to a 32×32 SRAM memory array.

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III EXISTING METHOD

Conventional SRAM uses the normal 6T SRAM cell configuration, whereby it is arranged in a memory array of 32×32, which utilizes row and column decoders, sense amplifiers, and precharge circuitry. The SRAM cells contain two inverters that are cross coupled and two access transistors to enable read and write operations, whereby writing and reading operations are performed through WL and BL & $B\overline{L}$.

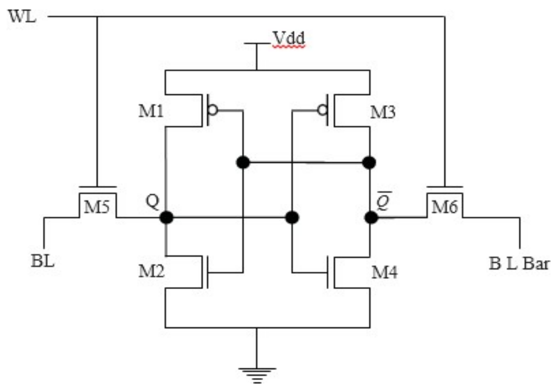

Fig 1: 6T SRAM cell

In write operations, data is written onto the memory cell by applying voltage to the bit lines while activating the word line. On the other hand, read operations use the sense amplifier to read data on the bit lines. The precharge circuit charges up the bit lines prior to each read operation to facilitate correct sensing.

The conventional 6T SRAM configuration is relatively simple in architecture and operates at high speed. Nevertheless, it exhibits high leakage power, especially during standby mode. Leakage currents increase as technology advances, thus raising the amount of static power consumed. Another disadvantage with the design is the lack of a power saving feature.

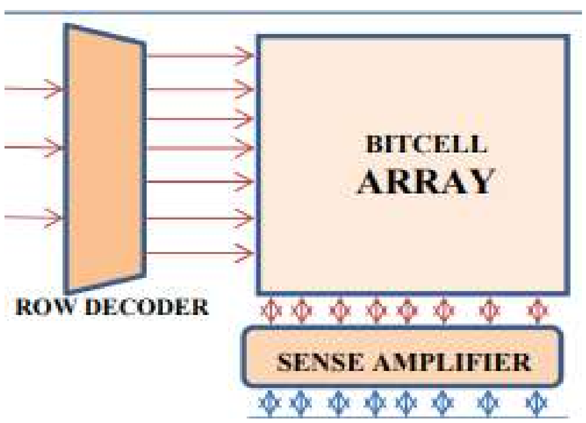

Fig 2: 6T SRAM of 32X32 array

IV PROPOSED METHODOLOGY

To circumvent the drawbacks associated with the traditional SRAM architecture, a low-power 32x32 SRAM memory array has been proposed by employing the power gating approach to efficiently minimize the leakage power when the SRAM is in standby mode. The suggested approach emphasizes sleep transistor integration with the typical 6T SRAM structure.

Proposed Design Overview

The proposed SRAM design includes:

- 6 Transistor SRAM cells in a 32x32 configuration
- Row/Column Decoding circuits
- Sense Amplifier circuit
- Precharge circuit
- Power Gating technique (sleep transistor)

The main goal is to achieve low standby power with proper read/write functionalities.

Power gating Technique

Power gating is a useful strategy to minimize leakage current in CMOS logic by isolating idle circuit blocks from the power source when not in operation. In the deep submicron domain, leakage currents, including subthreshold and gate currents, play a major role in determining total power dissipation, rendering power gating an appropriate method for designing low-power memory cells.

Power gating incorporates the use of a sleep transistor, usually a high-threshold voltage transistor, positioned between the power source and the circuit block. Depending on the location, power gating may be carried out using a header switch (PMOS) or a footer switch (NMOS). In this research, the header switch PMOS configuration is adopted owing to its superior leakage properties and noise resistance. During the active state, the sleep transistor is made "ON" which forms a direct connection between VDD and the SRAM array thus allowing read and write activities. During the standby state, the sleep transistor is made "OFF" thus disconnecting the memory array from the power source and decreasing the leakage current.

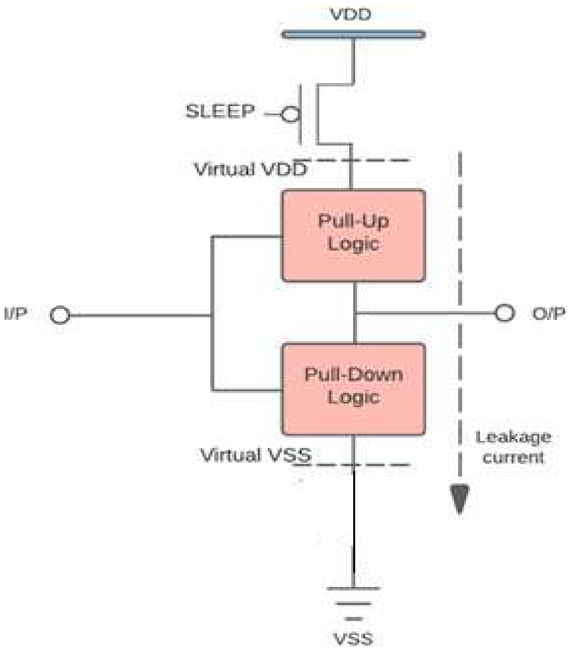

Fig 3: Block diagram of power gating technique.

Power gating requires correct transistor sizing to ensure optimal trade-offs between performance and reduced power consumption. Larger transistors result in lower voltage drop and higher speed but also lead to greater chip area. Besides, there will be a delay due to the transition between states of ON/OFF in case of timing requirements.

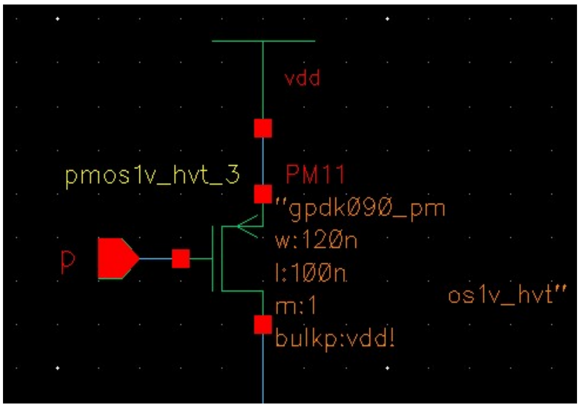

Fig 4: PMOS transistor for power gating.

In our proposed 32×32 SRAM array design, power gating is implemented through the PMOS sleep transistor. This allows for significant decrease in leakage power while not affecting the circuit performance significantly making this approach very attractive for power-limited systems.

Modified SRAM Architecture

This proposed SRAM structure can be said to be an improved version of the standard 32×32 SRAM circuit, whose constituent unit cells are made of the 6T SRAM cells, with modifications aimed at reducing the leakage current via the power gating approach. While the changes made in the former method involved changes in the internal circuitry of the cell itself, this approach does not change anything within the cell, and instead concentrates on the architectural improvements.

In this case, a PMOS header sleep transistor is placed between the power source and the SRAM circuit itself. The gate terminal of the sleep transistor is controlled by a particular signal line that indicates the state the memory has been put in. This approach allows for selectively disconnecting or connecting the memory array from the power source.

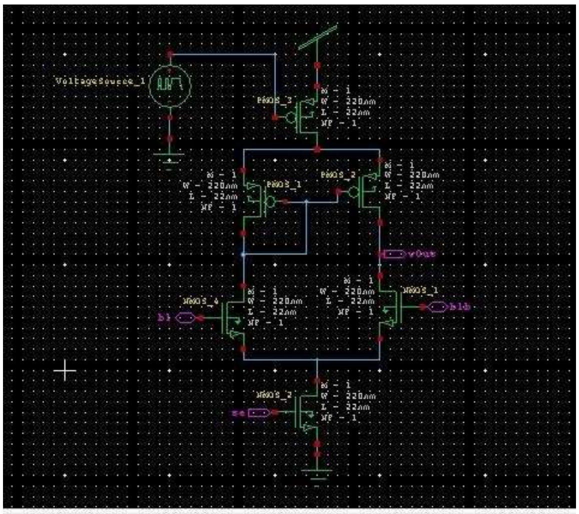

Fig 5: Power gated sense amplifier

The entire system is equipped with conventional peripheral circuits like row/column decoders, sense amplifiers, and pre-charging circuits for ensuring correct address decoding and reading/writing operations. In the active state, the sleep transistor stays ON to support the normal operations of the SRAM array. In the standby state, it gets switched off to isolate the array from VDD and thus cut off leakage power.

Power gating technology has been employed at the array level in order to avoid a high cumulative leakage power dissipated by several transistors without adding to the complexity of circuit design. It has also helped to simplify the task since it did not involve changes in the SRAM cells individually.

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Operations of proposed SRAM

The working mode of the power-gated 32 × 32 SRAM array design can be classified under three different states: writing state, reading state, and standby state. The introduction of the sleep transistor has not changed the characteristics of the basic 6T SRAM cells while in the active state.

Write Operation

During the write process, the information to be written is driven onto the bit lines (BL and $\overline{BL}$). The word line (WL) corresponding to this SRAM cell is enabled, causing the access transistors in that particular cell to become accessible.

- WL becomes enabled
- Information is driven on the BL and $\overline{BL}$
- SRAM cell gets its state changed

Since there is a sleep transistor present in the circuit, it does not matter in this case because it will stay in the ON position throughout the active mode.

Read Operation

During the read process, the bit lines are first charged with a higher voltage. With activation of the word line, the information held by the SRAM cell affects the voltage on the bit lines. The sense amplifier senses and amplifies the small voltage difference between BL and $\overline{BL}$ to give an output.

- Bit lines are precharged
- WL is enabled
- Information sensed and amplified

The proposed architecture guarantees reliable read operation since there is enough power supply from the gate transistor in active mode.

Standby Operation

For the standby state, the memory cell array is inactive, and power gating is enabled for reducing the leakage power. Sleep transistor is turned OFF to make the SRAM array in inactive state by cutting off the power supply.

- Sleep transistor OFF
- Power to array supply is cut off
- Leakage current minimized

Design implementation using Tanner EDA

This design concept is realized and simulated using Tanner EDA suite as follows:

S-Edit -> Designing SRAM cell and array schematically

T-Spice -> Simulating and analyzing the power consumption of the circuit

W-Edit -> Observing the waveforms

Design process consists of:

Designing the 6T SRAM cell

Designing the 32x32 memory array

Including peripheral circuits

Including a power gating transistor

Advantages of purposed method

- Reduction in leakage power is significant
- Provides stability in 6T SRAM cell
- Increase in transistor count is minimal
- Can be used for low power applications
- Minimized Effect on Thermal
- Minimized Area Cost
- CMOS Compatible
- Flexibility in Mode Control

V RESULTS AND DISCUSSIONS

Design and simulation of the proposed 32×32 SRAM memory array using the power gating technique have been carried out using Tanner EDA software. Performance analysis of the proposed design is done by comparing it with the conventional SRAM memory design based on power dissipation and circuit complexity.

The fallowing are the schematic designs of 32 x 32 SRAM memory array and peripheral circuits.

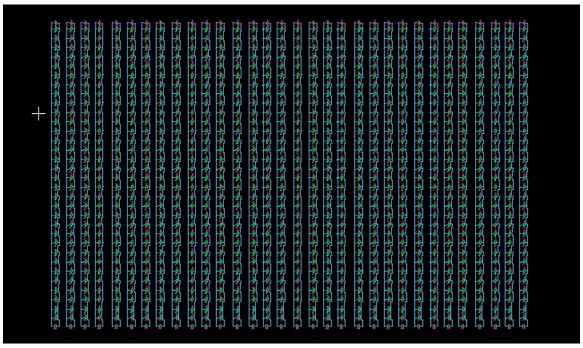

Fig 6: Schematic of proposed 6T SRAM of 32X32 array

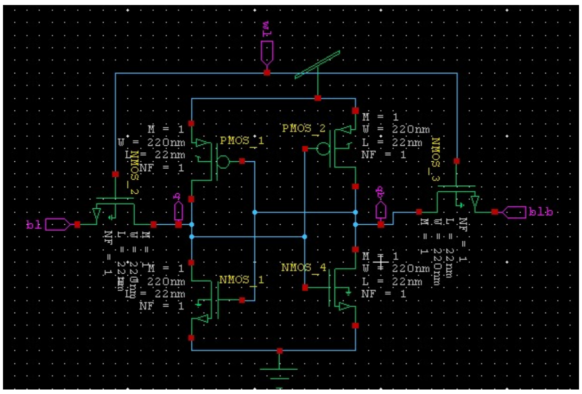

Fig 7: Schematic diagram 6t SRAM

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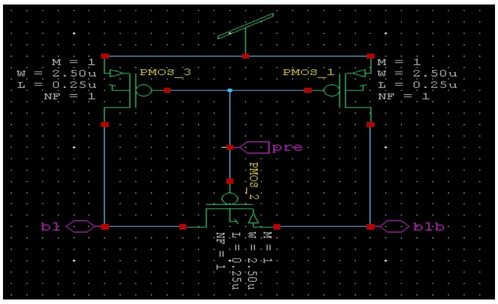

Fig 8: Schematic diagram pre charge.

Waveforms

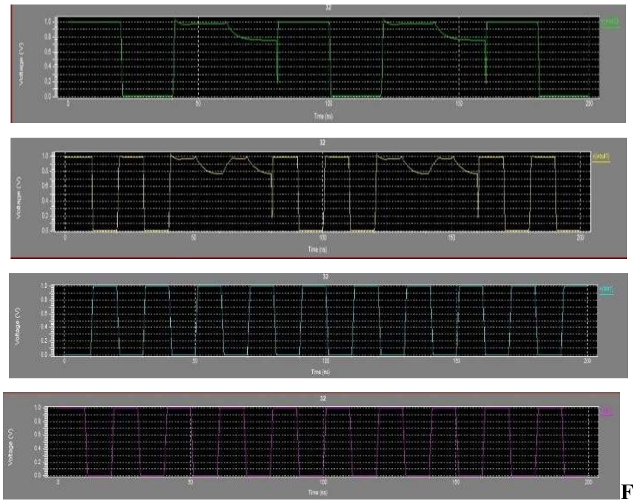

Fig 9: Waveforms of 32x32 sram array

Power Analysis

The main purpose of the proposed design is to minimize the leakage power when the device is idle. Simulation shows that there is a considerable decrease in power consumption.

Parameter	Conventional SRAM	Proposed SRAM
Power	2.615 µW	1.8402 µW
Mosfet count	6400	6432

Table 1: comparison table

Discussion of results

The reduction in power consumption is primarily due to the integration of the **power gating technique**, which effectively disconnects the SRAM array from the power supply during idle conditions. This minimizes leakage currents that dominate power dissipation in scaled CMOS technologies.

Despite the addition of a sleep transistor, the increase in transistor count is minimal and does not significantly impact the overall area. Moreover, the proposed design maintains stable read and write operations, as the sleep transistor is fully turned ON during active mode, ensuring proper voltage levels across the SRAM cells.

The simulation waveforms confirm correct functionality of the SRAM array in both active and standby modes. No significant degradation in performance is observed, indicating that the proposed method achieves an effective balance between power efficiency and operational reliability.

Overall analysis

It is evident that using power gating in a 32×32 SRAM cell is an effective strategy for implementing low-power designs. The suggested architecture effectively cuts down on standby power usage, while still retaining all the benefits of the existing 6T SRAM cell.

VI CONCLUSION

This work presents the implementation of a low-power 32×32 SRAM memory array that utilizes the concept of power gating in order to solve the problem of leakage power in deep sub-micron CMOS technology. In current VLSI circuits, leakage power forms one of the dominant sources of power dissipation, especially during standby mode operation, and hence techniques such as power gating become crucial for minimizing energy losses.

In this regard, the proposed memory design involves the use of a PMOS header sleep transistor alongside a standard 6T SRAM memory array. This ensures that the memory array can be selectively disconnected from the voltage supply when in an idle state and thus minimize the leakage power without changing the architecture of the SRAM cell itself.

A comprehensive design and simulation of the entire architecture of the SRAM, along with its peripheral circuits like decoders, sense amplifiers, and pre charging circuits, has been done using Tanner EDA suite. Both designs have been analyzed on similar parameters to compare the SRAM with the new power-gated SRAM circuit. From the simulation result, it can be seen that there is an effective reduction in power from 2.615µW to 1.7402µW, giving an increase of about 33% in leakage power reduction.

In addition to these, the proposed architecture also guarantees read/write operations while in active state due to proper conductance offered by the sleep transistor without causing a significant decrease in voltage level. Moreover, the effect of extra hardware added due to the introduction of sleep transistor on the size and complexity of the architecture is very low. The wake-up time is slightly higher during transitioning from standby state to active state.

From the findings of this paper, it can be concluded that using power gating on the array level is an effective and scalable technique for decreasing leakage power in SRAM-based memories. The technique is better than other techniques such as the increase in transistor numbers in the SRAM cell since it does not affect area efficiency and complexity of the design process.

In summary, the proposed power gated 32×32 SRAM structure is a good and effective design methodology for designing low-power SRAM memories. It is particularly suitable for energy constrained applications such as the Internet of Things (IoT), wearables, and biomedical systems.

VII FUTURE SCOPE

There are several approaches to improving the proposed power-gated 32×32 SRAM structure. These include incorporating more advanced SRAM cell configurations, including 8T or 9T cells, into the design to ensure that it remains stable and functional. Furthermore, the design can be scaled up to use for more significant memories and assess scalability.

Moreover, the optimization of sleep transistor sizing could result in lower wake-up times. Conducting implementation and simulations at the layout level will enable more precise results by accounting for practical issues during simulation.

The proposed technique can be combined with additional low-power designs to decrease power requirements even further. Moreover, the application of the proposed design in real-world environments can be used to test practicality. Real-time usage may involve implementing the technique in IoT or embedded systems applications.

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